LAYOUT

IC LAYOUT ENGINEER (REFERENCE: LE011)

Job Description:

- Candidate will be responsible for cell-level IC layout using Cadence and Mentor Graphics tool sets (Virtuoso Layout Editor, Assura, Calibre).
- Working on the development of predominantly RF/mixed-signal IC's with increasing levels of digital core integration against time.
- Will be responsible for automatic place and route layout techniques for some digital blocks using Encounter.
- Will work as part of a layout IC team on large projects.
- Will work closely with the IC design team throughout the design cycle to understand design requirements/layout constraints, and to support parasitic extraction, post layout verification and analysis.
- Will work closely with semiconductor foundries to submit the final GDSII and database and fill the required forms for the tape out

Required Skills:

- 0-2 Years of experience in IC layout and (or) CAD using Cadence and (or) Mentor layout tools.
- Good experience in automatic place and route (APR) is a plus.
- Experience with logic core standard-cell place and route is a must.
- Good knowledge of analog and RFIC layout techniques is a must.
- Good experience in state of the art technologies and deep sub-micron processes is a must.
- Shell scripting, Perl, and skill scripting knowledge are a plus.
- Good understanding of process design kit set-up and configuration for Mentor or Cadence based kits would be advantageous.

Qualifications:

- B.Sc. in Electronics Engineering.
- Excellent communications skills, written and spoken.
- Ability to work independently as well as a key team player.
- Oral and written fluency in English.

Interested candidates should send their resumes to careers@si-vision.com.
Please include "LE011_Name_GraduationYear" in the e-mail subject.

Silicon Vision
info@si-vision.com


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