DIGITAL DESIGN

AMS VERIFICATION ENGINEER, CONTRACT (REFERENCE DVP001)

Job Description:

As an AMS Verification Engineer, you will be responsible to verify advanced ASIC products that complement Silicon Vision AMS solutions. You are an Engineer who wants to contribute in the verification of key components of these ASICs, are excited by learning about new technologies, and are motivated by being part of a team that is critical to the success of Silicon Vision. You will be responsible to contribute to the verification strategy for ASIC projects and the documentation of the test plans, contribute to the development of ASIC verification infrastructure in System Verilog and UVM/OVM, and carry out verification tasks against the plan. You will write coverage models, and assertions, implement test-benches, write test cases to achieve coverage goals, and debug differences between implementation and reference models. You need to enjoy working in close collaboration with your colleagues.

Required Skills:

- BS in Computer Science, Electrical Engineering, Computer Engineering or equivalent
- BS in Computer Science, Electrical Engineering, Computer Engineering or equivalent
- A relevant industry experience verifying complex ASIC IPs and ASICs (desired)
- Key contributor to verification of at least one ASIC from project start to verification signoff and tape-out (desired)
- Excellent communication skills (both oral and written), problem solving skills, and a positive, team-oriented attitude, along with a desire to always learn something new
- Background and experience in implementing ASIC verification infrastructure in System Verilog and UVM (or OVM) and implementing assertions in SVA
- Experience in white-box/black-box testing strategies, defining, implementing, and achieving functional coverage and code coverage metrics
- Experience using, defining, and implementing revision control and issue tracking methodologies
- Experience in implementing automation using Python, Perl, C/C++, and TCL
- Knowledge of basic design concepts: Verilog based design, clock domain crossing, signaling protocols
- Exposure to writing reference models in Matlab/C/C++

Company Offers:

This is a contract based opportunity with 3 months of initial period and a possibility to extend.

Interested candidates should send their resumes to careers@si-vision.com.
Please include “DVP001" in the e-mail subject.

Silicon Vision
79 Almultaqa Alaraby,
Cairo, Egypt, P.O. Box 11361
Tel: +202-22669160
info@si-vision.com